L Number	Hits	Search Text	DB	Time stamp
1	739	(opening or recess or hole) and (pad with (etching or removing)) and (bump or solder) and @ad<=20010215	USPAT; US-PGPUB	2002/11/21 12:56
2	284	((opening or recess or hole) and (pad with (etching or removing)) and (bump or solder) and @ad<=20010215) and dielectric	USPAT; US-PGPUB	2002/11/21 12:50
3	4	(opening or recess or hole) and (pad with (etching or removing)) and (bump or solder) and dielectric	EPO; JPO; DERWENT; IBM_TDB	2002/11/21 12:56

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TITLE: Reliable metal bumps on top of I/O pads with test probe marks

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The process starts with a semiconductor surface 10, FIG. 1, typically the surface of a silicon single crystalline substrate. A layer 13 of Intra Metal Dielectric (IMD) is deposited over the surface 10. A layer 17 of metal, typically aluminum, has been deposited over the surface of the layer 13 of IMD. Layer 17 of aluminum is patterned and etched typically using a layer of photoresist (not shown in FIG. 1) and conventional methods of photolithography and etching. After the bond pad 17, FIG. 2, has been created in this manner, a layer 11 of passivation is deposited over the layer 13 of IMD. An opening 15 that aligns with the bond **pad** 17 is created in the layer 11 of passivation, again using methods of photolithography and **etching**.

The removal of region 36, FIG. 8b, which will be further highlighted in FIGS. 9 through 11, can be summarized as being performed by depositing a layer of photoresist over the surface of the aluminum **pad** (typically this implies the deposition of a layer of photoresist over the surface of the entire wafer after wafer level testing has been completed), patterning and **etching** the layer of photoresist thereby creating openings in the layer of photoresist that align with region 36 for all aluminum pads on the surface of the wafer that have been used as I/O contact points by a tester probe, and **removing** the aluminum in accordance with the openings that have been created in the layer of photoresist. This latter removal (etching) of the aluminum can be performed using conventional methods of etching aluminum such as plasma enhanced dry

etching or wet etching with a H.sub.3 PO.sub.4 solution. These and other processing steps, which relate to the creation of the reliable metal bump of the invention, are further highlighted in the following drawings.

The layer 37 of photoresist will, after patterning and **etching,** remain in place in an area above the aluminum **pad** 24 that surrounds the probe mark 28 in the surface of aluminum **pad** 24. The deposited layer 37 of photoresist can, prior to patterning and etching, be cured or pre-baked further hardening the surface of the layer 37 of photoresist.

The **etching** of the aluminum **pad** 24 in accordance with opening 31 can, as previously stated, use methods of plasma enhanced dry **etching** or wet **etching** with a H.sub.3 PO.sub.4 solution. Other methods for the **etching** of the aluminum **pad** have previously been highlighted and equally apply at this stage in the process.

1. A method for forming a metal bump on a semiconductor surface, comprising the steps of: providing a semiconductor surface, said semiconductor surface having been provided in or on the surface thereof with a contact pad, said contact pad sitting on an underlying layer of dielectric and being in electrical contact with at least one point of electrical contact in or on the surface of said substrate; depositing a layer of passivation over the surface of said layer of dielectric underlying the contact pad, including the surface of said contact pad; patterning and **etching** said layer of passivation, creating an opening in said layer of passivation having a first diameter, partially exposing the surface of said contact **pad** over a surface area of said first diameter, said first diameter of said opening created in said layer of passivation being smaller than a surface area of said contact **pad** by a measurable amount; patterning and **etching** said contact **pad,** creating an opening in said contact **pad** having a second diameter, said second diameter of said opening in said contact **pad** being smaller than said first diameter of said opening in said layer of passivation by a measurable amount; sputtering a layer of Under Bump Metallurgy (UBM) over the surface of said layer of

passivation, including exposed surface of the contact pad and exposed surface of the underlying dielectric; depositing and patterning a layer of photoresist, creating an opening in the photoresist with a slightly larger dimension than said first diameter; electroplating a layer of bump metal in the photoresist opening; stripping the layer of photoresist and etching said layer of UBM, using said layer of bump metal as a mask; and reflowing the surface of said layer of bump metal, forming the metal bump.

10. A method for forming a metal bump on a semiconductor surface, comprising the steps of: providing a semiconductor surface, said semiconductor surface having been provided in or on the surface thereof with a contact pad, said contact pad overlying and being in electrical contact with at least one point of electrical contact in or on the surface of said substrate, said at least one point of electrical contact being created on the surface of a layer of dielectric, said layer of dielectric having been deposited over said semiconductor surface; and partially **removing** said contact **pad, said removing** having a removal thickness and removal surface area.

14. The method of claim 10 wherein said partially **removing** said contact **pad** comprises the steps of: depositing a layer of passivation over the surface of said layer of dielectric, including the surface of said contact **pad**; patterning and **etching** said layer of passivation, creating an opening in said layer of passivation having a first diameter, partially exposing the surface of said contact **pad** over a surface area of said first diameter, said first diameter of said opening created in said layer of passivation being smaller than a surface area of said contact **pad** by a measurable amount; and patterning and **etching** said contact **pad** creating an opening in said contact **pad** having a second diameter, said second diameter of said opening created in said contact **pad** being smaller than said first diameter of said opening created in said layer of passivation by a measurable amount.

24. A method for forming a metal bump on a semiconductor surface, a layer of dielectric having been deposited over said semiconductor surface, said contact

pad having been formed on the surface of said layer of dielectric, said metal bump overlying said contact pad, said contact pad having served as an Input/Output (I/O) point of contact during semiconductor device testing, said contact pad overlying and being connected to at least one point of electrical contact provided in or on the surface of said semiconductor surface, comprising the steps of: depositing a layer of passivation over said layer of dielectric underlying said contact pad, including the surface of said contact pad; patterning and **etching** said layer of passivation, creating an opening in said layer of passivation having a first diameter, partially exposing the surface of said contact **pad** over a surface area of said first diameter, said opening in said layer of passivation being centered with respect to said contact **pad,** said first diameter of said opening created in said layer of passivation being smaller than said surface area of said contact **pad** by a measurable amount; depositing a first layer of photoresist over the surface of said layer of passivation, including the opening created in said layer of passivation; patterning and **etching** said first layer of photoresist, creating an opening having a second diameter through said layer of photoresist, said opening in said first layer of photoresist aligning with and being centered with respect to said contact **pad,** said second diameter of said opening in said first layer of photoresist being smaller than said first diameter of said opening in said layer of passivation by a measurable amount; **etching** said contact **pad in accordance with said opening** created in said first layer of photoresist; **removing** said patterned layer of first photoresist from the surface of said layer of passivation, including the surface of said etched contact **pad;** sputtering a layer of Under Bump Metallurgy (UBM) over the surface of said layer of passivation, including exposed surface of the contact pad and exposed surface of said underlying dielectric; depositing a second layer of photoresist over the semiconductor surface of the layer of UBM; patterning and **etching** said second layer of photoresist, creating an opening in said second layer of photoresist that is aligned with said contact **pad,** partially exposing the surface of said layer of UBM; electroplating the partially exposed surface of said layer of UBM with a layer of bump metal, partially filling said opening created in said second layer of photoresist; removing said patterned and

etched second layer of photoresist from above said semiconductor surface; and reflowing the surface of said layer of bump metal, forming the metal bump.

35. The method of claim 24 wherein said **etching** said contact **pad in accordance with said opening** created in said first layer of photoresist comprises methods of plasma enhanced dry **etching** or wet **etching** with a H.sub.3 PO.sub.4 solution.

36. The method of claim 24 wherein said **etching** said contact **pad in accordance with said opening** created in said first layer of photoresist comprises **etching** AlCu using Cl.sub.2 /Ar as an etchant at a temperature between 50 and 200 degrees C., an etchant flow rate of about 20 sccm for the Cl.sub.2 and 1000 sccm for the Ar, a pressure between about 50 mTorr and 10 Torr, a time of the etch between 30 and 200 seconds.

38. A metal bump on a semiconductor surface, comprising: a semiconductor surface, a layer of dielectric having been deposited over said semiconductor surface, a contact pad having been formed on the surface of said layer of dielectric, said metal bump overlying said contact pad, said semiconductor surface having been provided with at least one point of electrical contact, said contact pad having a surface area in addition to having a height in addition to having a surface area, said contact pad being in electrical contact with said at least one point of electrical contact; and said contact **pad** having been partially removed, said **removing** having a removal thickness and removal surface area.

65. A method for forming a metal bump on a semiconductor surface, comprising the steps of: providing a semiconductor surface; providing a contact pad over said semiconductor surface; mechanically contacting a portion of said contact pad, whereby damage may occur to said portion of said contact pad; **removing** said portion of said contact **pad** to form an opening; depositing an under bump metal over said contact pad and in said opening; and forming a metal bump over said contact pad.